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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,891	01/21/2004	John Atkinson Fifield	BUR920030077US1	1890

42640 7590 04/18/2005

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EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/707,891	FIFIELD ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-15* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application No. 10/707,891 filed on 01/21/04. Claims 1 – 15 are pending on this application.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> ((b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States

4. Claims 1 – 9, and 11 are rejected under 35 U.S.C. 102(b) as being anticipate by Chen U.S. patent No. 6,194,962.

Regarding claim 1, Fig. 4 of Chen discloses a differential amplifier circuit comprising: a first differential amplifier (MN1, MN2) for receiving a pair of differential input signals (Vin+, Vin-) to generate a first output (Ioutn); a second differential amplifier (MP1, MP2) for receiving said pair of differential input signals

(Vin+, Vin-) and generate a second output (Ioutp) and a summing circuit (34) for summing said first output (Ioutn) of said first differential amplifier (MN1, MN2) and said second output (Ioutp) of said second differential amplifier (MP1, MP2) to provide a common output (Iout) for said differential amplifier circuit .

Regarding claim 2, wherein said first differential amplifier is an n-channel differential amplifier (MN1, MN2).

Regarding claim 3, wherein said first differential amplifier (MN1, MN2) includes a pair of n-channel transistors (MN1, MN2) for receiving said pair of differential input signals (Vin+, Vin-), respectively.

Regarding claim 4, wherein said second differential amplifier (MP1, MP2) is a p-channel differential amplifier.

Regarding claim 5, wherein said second differential amplifier (MP1, MP2) includes a pair of p- channel transistors (MP1, MP2) for receiving said pair of differential input signals (Vin+, Vin-), respectively.

Regarding claim 6, wherein said summing circuit (62) is an n-channel filter differential amplifier (Summing circuit 34 discloses a pair of n-channel transistor Bias2 filter).

Regarding claim 7, wherein said summing circuit (34) includes a pair of n-channel transistors (of n-channel transistor Bias2) for receiving a voltage reference signal (pos/neg trimming signal in reference to Ioutn, Ioutp) said first output (Ioutn) of said first differential second output (Ioutp) of said second differential amplifier.

Regarding claim 8, wherein said differential circuit further includes a reference volt-age generation circuit (MP3, MP4) for providing said reference voltage (POS TRIM, NEG TRIM) for said summing circuit (34).

Regarding claim 9, wherein said voltage reference circuit (MP3, MP4) includes a differential amplifier (MN1, MN2) having inputs connected to an output (loutn) of said differential amplifier (MN1, MN2).

Regarding claim 11, wherein said summing circuit (34) receives an active low ENABLE-P signal (Vbias1).

5. Claims 1 and 10 are rejected under 35 U.S.C. 102(e) as being anticipate by Wu et al. U.S. Patent No. 6,590,432.

Regarding claim 1, Fig. 4 of Wu et al. discloses a differential amplifier circuit (80 comprising: a first differential amplifier (72, 74) for receiving a pair of differential input signals (VP, VN) to generate a first output (DOP); a second differential amplifier (78, 76) for receiving said pair of differential input signals (VN, VP) and generate a second output (DON) and a summing circuit (70) for summing said first output (DOP) of said first differential amplifier (72,74) and said second output (DON) of said second differential amplifier (78, 76) to provide a common output (DOP, and DON of 70) for said differential amplifier circuit (80).

Regarding claim 10, wherein said first (72, 74) and second (78, 76) differential amplifiers receive and active low enable signal (PBIAS of 64).

6. Claims 1, 13, 14, and 15 are rejected under 35 U.S.C. 102(b) as being anticipate by Tai U.S. Patent No. 6,507,245.

Regarding claim 1, Fig. 3 of Tai discloses a differential amplifier circuit comprising: a first differential amplifier (S1, S2) for receiving a pair of differential input signals (input signals at the gates of S1 and S2) to generate a first output (N4); a second differential amplifier (Q1, Q2) for receiving said pair of differential input signals (input signals at the gates of Q1 and Q2) and generate a second output (N3) and a summing circuit (52, 62) for summing said first output (N4) of said first differential amplifier (S1, S2) and said second output (N3) of said second differential amplifier (Q1, Q2) to provide a common output (N2) for said differential amplifier circuit (40).

Regarding claim 13, wherein said first differential amplifier (S1, S2) receives a gate control voltage (Vg2) to control the current through an n channel transistor (S5) within said first differential amplifier (S1, S2) in a consistent and predictable manner using a current mirror technique (S3, S4).

Regarding claim 14, said second differential amplifier (Q1, Q2) receives a gate control voltage (Vg1) to control the current through a p-channel transistor (Q5) within said second differential amplifier (Q1, Q2) in a consistent and predictable manner using a current mirror technique (Q4, Q3).

Regarding claim 15, wherein said summing circuit (52, 62) receives a gate control voltage (Voltage at the gate of Q7) to Control the current through an n-channel transistor (Q) within said summing circuit (62) in a consistent and predictable manner using a current mirror technique (Q9, Q10).

Allowable Subject Matter

7. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach, wherein the summing circuit includes a clamp device to hold the common output high when said ENABLE-P signal is low.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

4/14/05

Linh Van Nguyen

Art Unit 2819